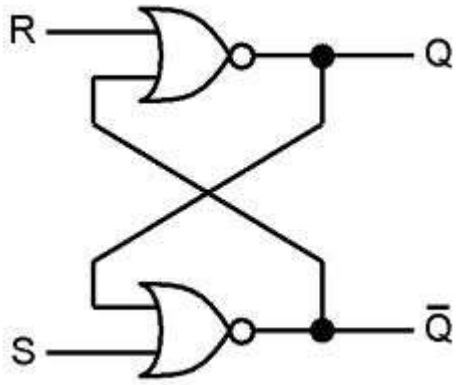
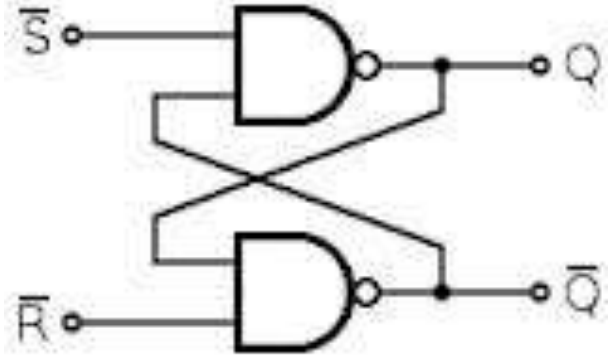
Lecture 7: Latches

1. Combinational circuits can be described by Boolean expressions where the output is strictly dependent on only the inputs.
2. Sequential circuits depend not only on the current inputs, but also on the history of inputs, i.e. they have a memory.
   2.1. The history of inputs determines the "state" of the circuit.
   2.2. Examples: house alarm system that must be reset once it senses an intrusion, or a combination lock.
3. Latch = a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.
4. SR Latches = a sequential circuit that has two inputs, Set that sets the latch and Reset that clears the latch, and two complementary outputs. Unlike the combinational circuits, the outputs of the latch are not uniquely determined by the current inputs.



S-R NOR Latch



S-R NAND Latch

4.1. Characteristic Tables

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Undefined

S-R NOR Latch

S	R	$\overline{S}$	$\overline{R}$	Q_{n+1}
0	0	1	1	Q_n
0	1	1	0	0
1	0	0	1	1
1	1	0	0	Undefined

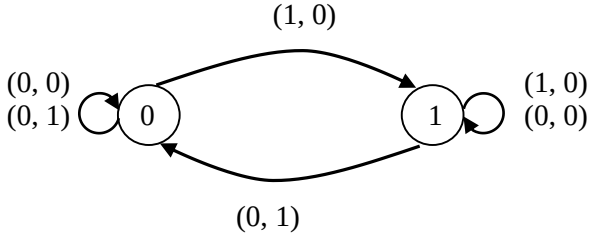
S-R NAND Latch

4.2. State Transition Table for S-R NOR Latch

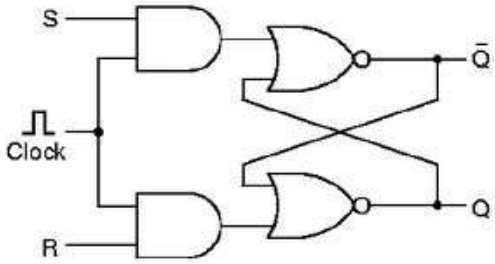
Present Inputs		Present State	Next State	Type of circuit
S	**R**	**Q**	**Q'**	
0	0	0	0	Memory
0	0	1	1	Memory
0	1	0	0	Combinational
0	1	1	0	Combinational
1	0	0	1	Combinational
1	0	1	1	Combinational
1	1	0	?	Combinational
1	1	1	?	Combinational

4.2.1. For NOR Latch inputs (1,1) the later states become unpredictable
4.2.2. For AND Latch inputs (0,0) later states become unpredictable.

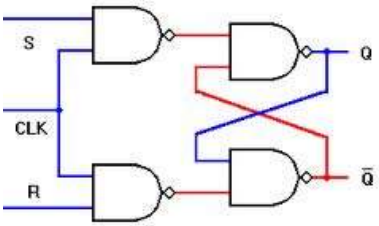
4.3. State Transition Diagram for Q and combinations of (S,R)



5. Clocked S-R Latch used to prevent the latch from changing except at specific times by adding AND gates in front of the inputs.

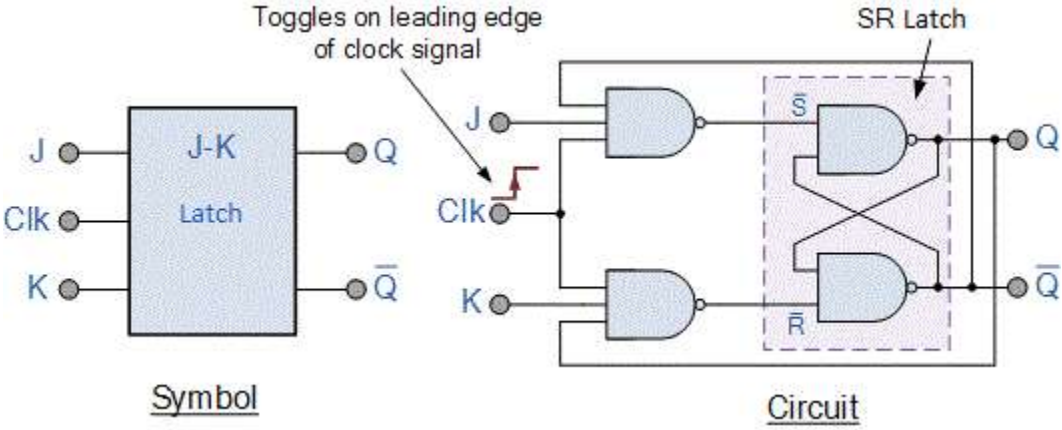


Clocked S-R NOR Latch

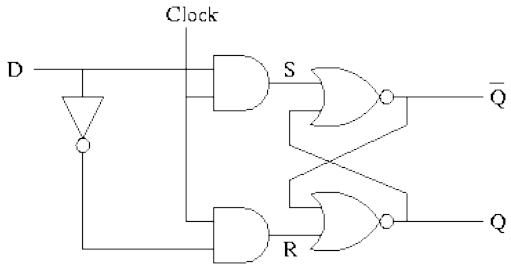


Clocked S-R NAND Latch

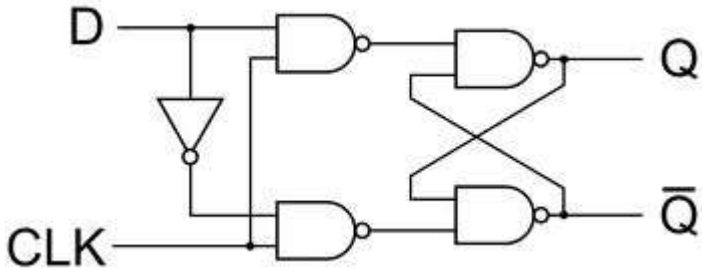
6. Clocked J-K Latch that uses feedback from outputs to achieve toggle.



7. Clocked D Latch takes only one input and ensures that inputs that cause unpredictable states can never occur.
   7.1. The output of a D flip-flop is always equal to the most recent value applied to the input.
   7.2. When the clock is 1, the current value of D is sampled, and stored in the latch. The value stored is always available at Q.

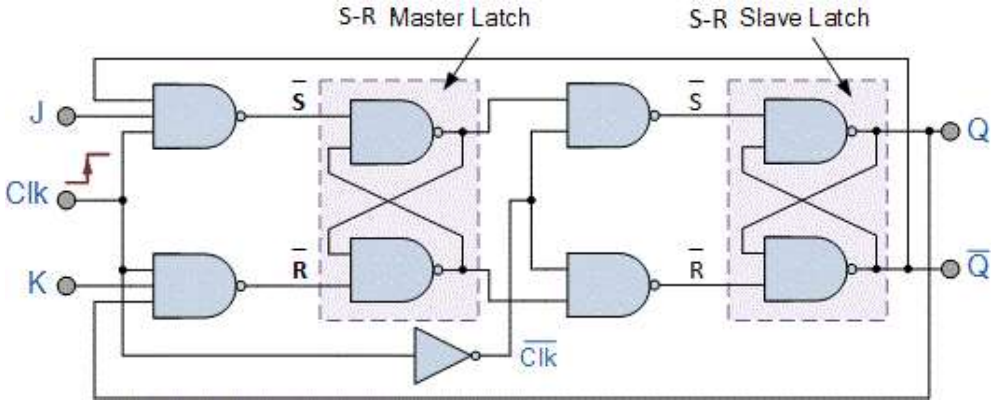


Clocked NOR D Latch



Clocked NAND D Latch

8. J-K Master-Slave Flip-Flop



When the clock is HIGH, the master latch circuit accepts values from the input, and, because of the clock inverter, the slave latch is unchanged. When the clock becomes LOW the slave accepts the now fixed value from the master circuit. This makes the entire circuit a "flip flop" because it only changes on the falling edge of the clock signal rather than a clock level.