1. Programmable Logic Devices (PLD) = any type of IC implementing digital hardware where the chip can be configured by the end user to realize different designs
   1.1. Programmable Logic Array (PLA) = a small PLD that contains two levels of logic, and AND-plane, and an OR-plane, where both levels are programmable.
      1.1.1. Field Programmable Logic Array = every possible connection is made through a fuse at every interconnection point, and then later removed by blowing the fuse.
      1.1.2. Applying a mask during chip fabrication by using an appropriate mask supplied for a particular chip fabrication.

2. Building a Computer from parts.
   2.1. They now know enough to build a computer.
   2.2. Add two numbers => switches -> full adder -> LEDs
   2.3. Add, OR, or AND two numbers => switches -> ALU.circ -> LEDs
   2.4. Calculate running sum => switches -> storage <-> ALU.circ + more states -> LEDs
   2.5. Add based on values stored somewhere => switches -> storage + input register <-> ALU.circ + more states -> LEDs
   2.6. We want computer to
      2.6.1. Move Data In/out of machine (input regs)
      2.6.2. Process Data ALU
      2.6.3. Store Data Accumulator
      2.6.4. Control Switches
   2.7. Storage
      2.7.1. Some storage in CPU registers, not much but what is there is very close.
      2.7.2. Cache
      2.7.3. There is some storage external as well (RAM).
      2.7.4. Secondary is very far away (I/O) and very slow.
   2.8. Add 2 registers to our machine need one of two things
      2.8.1. we either need direct paths from the ALU to the registers,
      2.8.2. A bus is a collection of low-resistance wires, used to facilitate the transfer information from one place to another is a computer. Think of streets - each house could have a separate path to the store (or each dorm room could have a separate path to the bar) but it is more efficient to share the path (streets, for example). A bus often has data lines, address lines, and control lines. Inside the CPU the bus only contains the data lines, while the control and address lines are routed separately. This is where 3-8 and 4-16 decoders come in real handy.
      2.8.3. Still non-von Neuman because there is no stored program.
   2.9. Given registers are connected to a BUS, and are D FF's, what else do we need? A register will load from either the bus or some other place (I/O, for example).
      2.9.1. Need control lines to select which to load from.
      2.9.2. Also need addresses (which register is to be loaded, for example). Technically address lines are also control lines, since they help the logic control which register is to be operated on. (Clocks into DFF can be anded with decoded address line to cause value to be loaded. This is not actually done for a variety of reasons.)