Chapter 2: Computer Organization

I. Main Memory Organization and Major Hardware Components

A. What is the type of information stored in a memory location?
   1. Unknown by hardware.
   2. It is in the hands of the programmer/compiler.
      a) int y = -32697; /* 0x8047 */
      b) printf("%d %u %c\n", y, y, y); /* in a 32 bit machine: */
      c) -32697 32839 G in a 32 bit

II. Main Memory Organization

A. word size = usually the size of number used in CPU addition circuitry. 32 bits usually now. Integers the size of a word.
B. How are multiple byte words stored?
   1. Little-endian. LSByte has lower address. Intel.
   2. Big-endian. LSByte has highest address. VAX, SPARC, CUSP.
      a) Allows word subtraction for alphabetizing.
   3. MIPS and PowerPC give the OS the choice of either endian when it boots.
C. Words must be aligned in most machines. In 32-bit, means words only begin at addresses which are multiples of 4.
   Thus byte access and word access are two different things.
D. Most RISC machines tend to use fixed instruction length equal to the word size.
E. Most CISC machines have variable instruction lengths, 1 - 6 bytes or more.
F. address size = number of bits in an address. CUSP 12 bits, 8086 20 bits, 286 24 bits, 386+ and RISC 32 bit.

III. Four Major Hardware Components of a Computer

A. CPU
   1. ALU = arithmetic and logic unit. Arithmetic, bitwise operations, compare. Doesn't store anything.
   2. Control Unit is intelligence of CPU. Does decoding.
   3. Registers
      a) PC = Program counter. Contains address of currently executing instruction.
      b) On Intel actually CS (code segment) and IP (instruction pointer).
         1) 16-bit mode has 20 bit addresses, uses 16 bit CS as MSB and then adds 16 bit IP.
         2) 32-bit mode has 32 bit addresses uses 32 bit CS and IP.
      c) SP = Stack pointer. Contains address of top of stack for temporary storage.
      d) XR = Index register. Helps access arrays.
      e) PS = Process status register. Contains flags, including condition codes and big-endian vs little endian flag for PowerPC and MIPS.
         1) CUSP flags: OV = overflow, LT = less than, EQ = equal, IE = interrupt enabled.
f) DRs = Data registers.
   (1) Word size
   (2) CUSP: Accumulator
   (3) Intel P4 has 8, and 8 SIMD registers. AMD64 has 16 data, and 16 SIMD registers.
   (4) MIPS has 32 32-bit general purpose registers + PC and two for multiplication
   (5) SPARC has 8 global and a register window onto a "register file" of up to 128 registers that sees 24
       registers at a time. There are 8 local registers, and 8 registers overlap with each of the adjacent windows.
       Implementations allow 2 to 32 windows. Great for procedure calls. Think of as top of stack.

g) MAR = Memory address register. CPU connection to address bus.
h) MDR = Memory data register. CPU connection to data bus.
i) IR = Instruction register. Holds current instruction, so MDR may be overwritten.

4. Memory
   a) Internal cache on CPU Chip.
   b) Pentium 8K data, 8K address
   c) Secondary Cache on motherboard before system bus. 256K - 1M; 15 ns

B. Main memory on motherboard 60 ns
   1. Secondary Memory on disk 10000 ns

C. I/O Devices
   1. Keyboards, monitors, CD-ROMs, modems, printers, modems, floppy disks, hard disks

D. System Bus
   1. Data Bus-Same number of lines as bits in a memory word.
      a) CUSP 24 bits
      b) Pentium 2 * 32-bits allows two words to be accessed simultaneously.
   2. Address Bus-Same number of lines as bits in the computer's addresses
      a) CUSP 12 bits

3. Control Bus
   a) MEMR and MEMW tell memory whether to read or write.

IV. Instruction Cycle-Fetch, decode, execute.
   A. Fetch by transferring instruction at address of PC from memory to IR. IR = Memory[PC]
   B. Decode instruction using microcode of CPU.
      1. Also increment PC. PC = PC + 1
   C. Execute the instruction.

V. Self-Modifying Programs
   A. The only thing to be learned from these is that code and data are indistinguishable to the computer.